

MS-7676 Ver: 4.1 m-ATX : 245 X 245mm

CPU:

INTEL - Sandy Bridge LGA 1155

System Chipset:

INTEL - Cougar Point PCH(Z68/H67)

OnBoard Chipset:

HD Audio Codec:RTL887 Co-lay 892

LAN:RTL 8111E 10/100/1000 , Co-lay 8105E 10/100

SIO:FIN71869AD

Flash ROM: 32Mb SPI (PCH)

Main Memory:

DDRIII (1066/1333MHz) * 2 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 2

PCI Express (X1) Slot * 2

PWM:

Controller:VRD12 Ut501 3Phase

CPU+GPU: UP6282 MOSFET Driver

CPU VTT: UP6103 A

CPU SA : OP+MOS

DDR: UP6103A

PCH: UP6103A

ACPI:

UPI

Other:

SATA3.0 x2 + SATA2.0 x4 (PCH)

USB2.0 RearX4 Front x6

USB3.0 RearX2

D-SUB/DVI/HDMI *1

TPM Header *1(debug only)

on BOARD BUZZER

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兩個BOM:

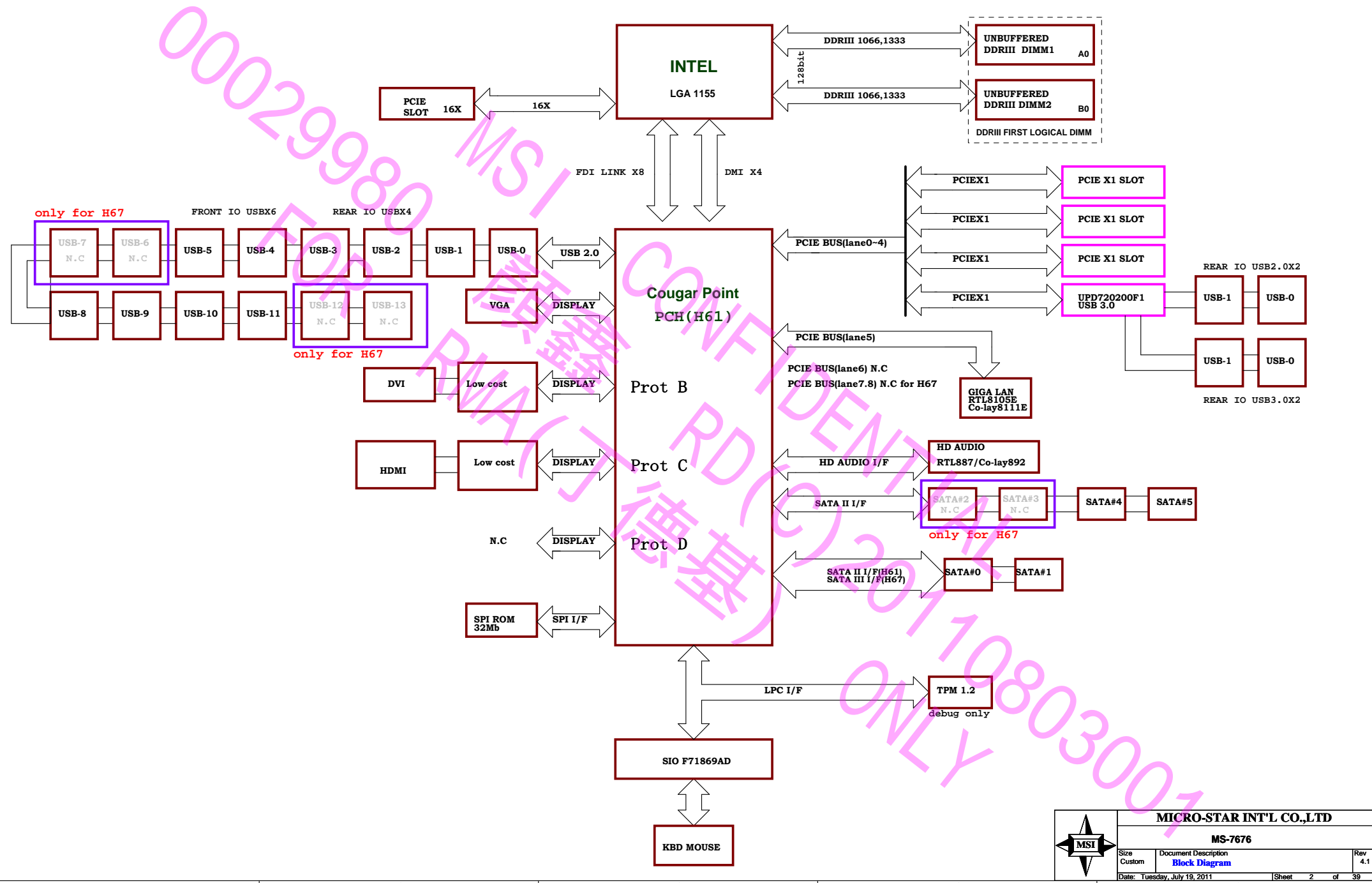
1. Z68
2. H67



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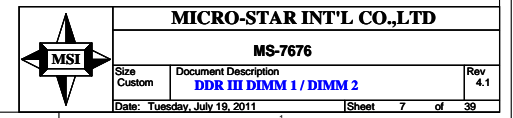
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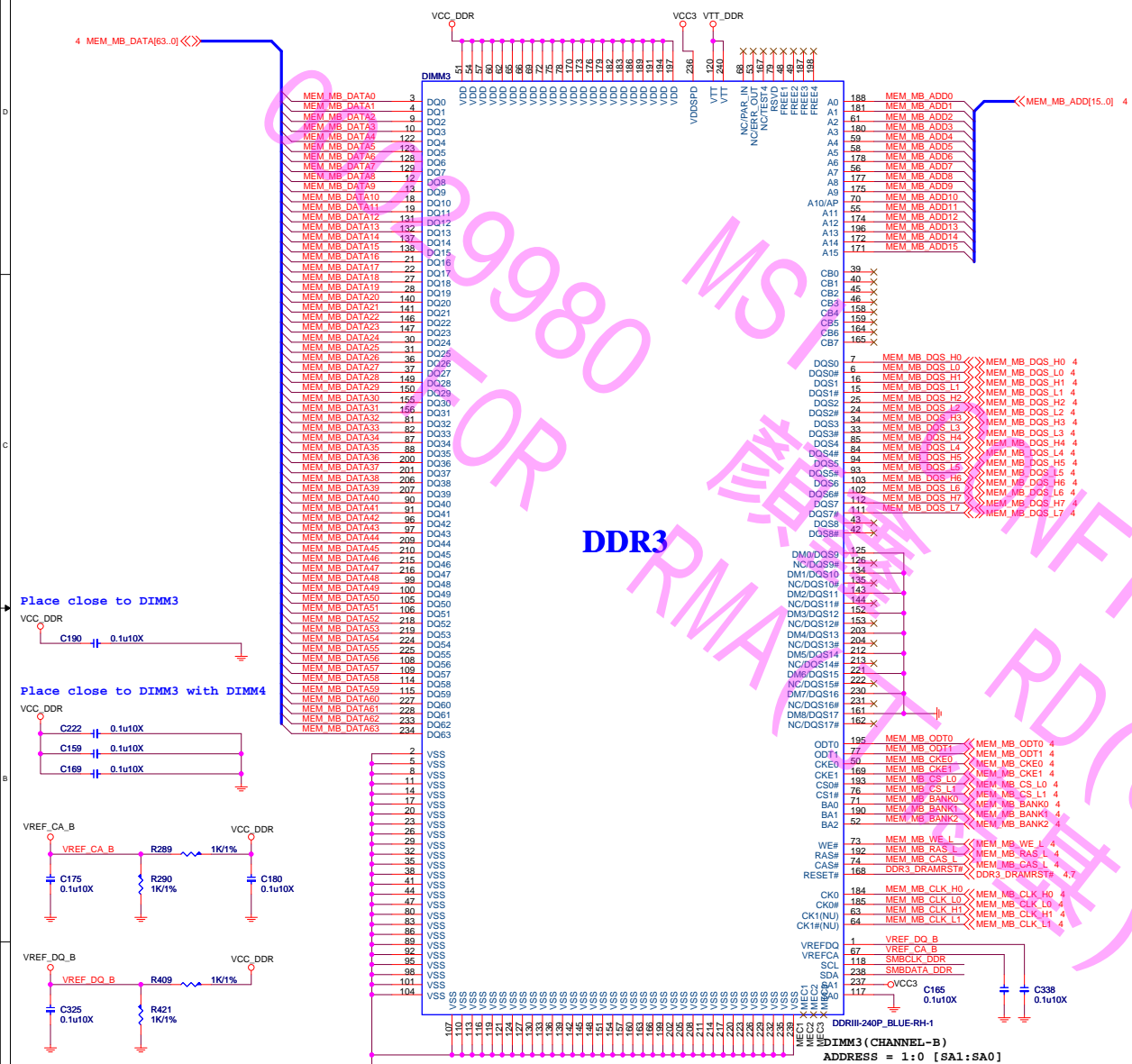




DDRIII DIMM_A1

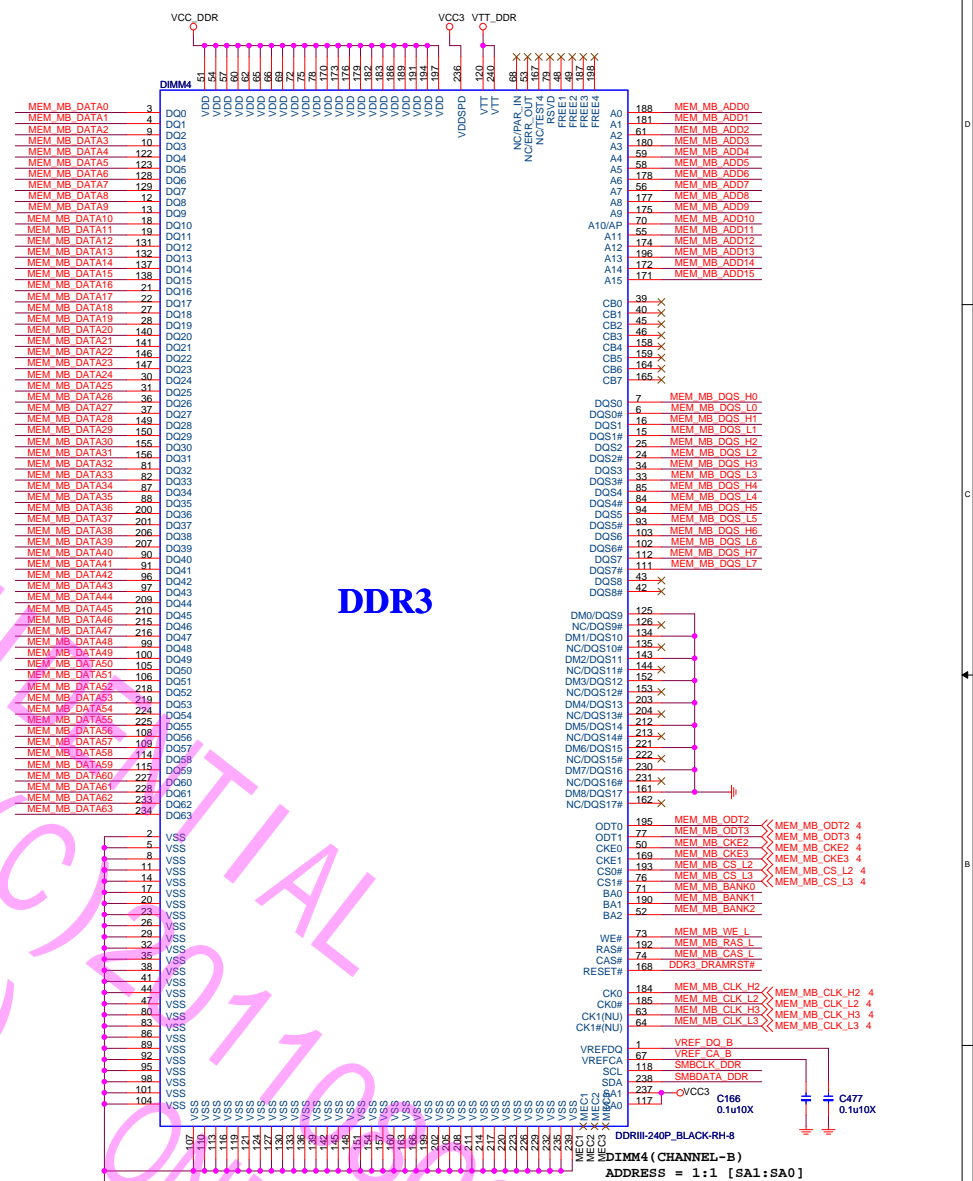


DDRIII DIMM_B0



DDR3

DDRIII DIMM_B1



DDR3

SMBCLK_DDR << SMBCLK_DDR 7
SMBDATA_DDR << SMBDATA_DDR 7



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REQUIRED STRAPS

Internal pull-up
Internal pull-up

BM_BSY# R529 10K/1%
LPC_DRQ#0 R714 X 10K
LPC_DRQ#1 R702 X 10K
STP_PC# R622 X 10K
SMBCLK R666 1.8K
SMBDATA R667 1.8K
FP_RST# R562 10K/1%
PCH_GPIO35 R624 X 10K

FP_RST# R564 X 10K/1%
SIO_PME# R703 10K/1%
SPL_HOLD_GPO# R641 X 10K/1%
PCIECLKREQ2# R575 X 10K/1%
PCIECLKREQ5# R642 X 10K/1%
PCIECLKREQ6# R547 X 10K/1%
PCIECLKREQ7# R645 X 10K/1%
SPL_LANE# R647 X 10K/1%
PCH_GPIO24 R655 X 220R
PCH_GPIO28 R623 X 10K/1%

PCH_GPIO72 R538 10K/1%
SB_WAKE# R636 1K
Ri# R658 10K/1%
SMLINKO_CLK R668 10K/1%
SMLINKO_DATA R669 10K/1%
PCH_SML0ALERT# R660 10K/1%
PCH_SML1CLK# R659 10K/1%
PCH_SML1DATA R674 10K/1%
PCH_SML1ALERT# R697 10K/1%
SMBALERT# R698 10K/1%

SUSWARN#_CP R682 X 0R
RSMRST# R606 X 0R

SUSACK#_CP R682 X 0R
RSMRST# R606 X 0R

PCH_GPIO31 R675 10K/1%
PCH_GPIO27 R762 10K/1%
SUSACK#_CP R16 10K
DPWROK_CP R25 10K

PCIECLKREQ2# R574 10K/1%
PCIECLKREQ5# R634 10K/1%
PCIECLKREQ6# R539 10K/1%
PCIECLKREQ7# R640 10K/1%
PCH_GPIO33 R717 X 1K

PCIECLKREQ can't find 0/1/3/4

SUSWARN#_CP R682 X 0R
RSMRST# R606 X 0R

SUSACK#_CP R682 X 0R
RSMRST# R606 X 0R

SUSACK#_CP R682 X 0R
RSMRST# R606 X 0R

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RSMRST# R606 X 0R

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RSMRST# R606 X 0R

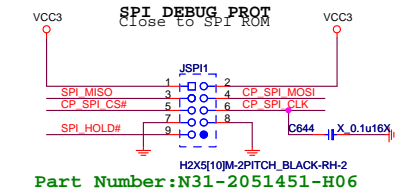
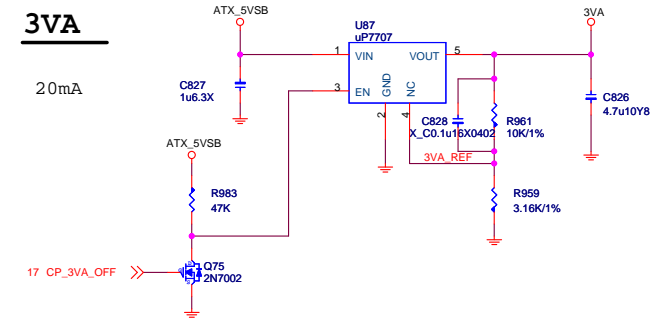
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RSMRST# R606 X 0R

SUSACK#_CP R682 X 0R
RSMRST# R606 X 0R



3VA

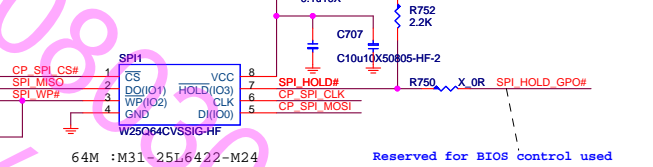
20mA



Part Number: N31-2051451-H06

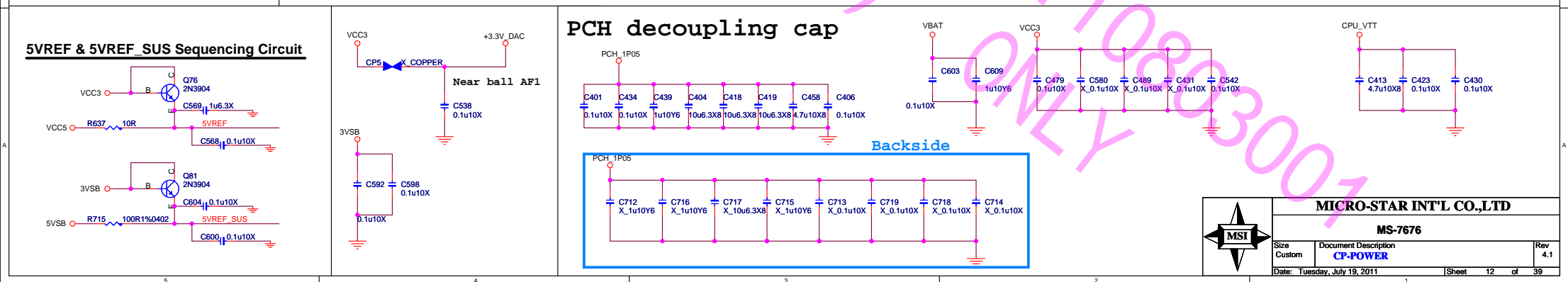
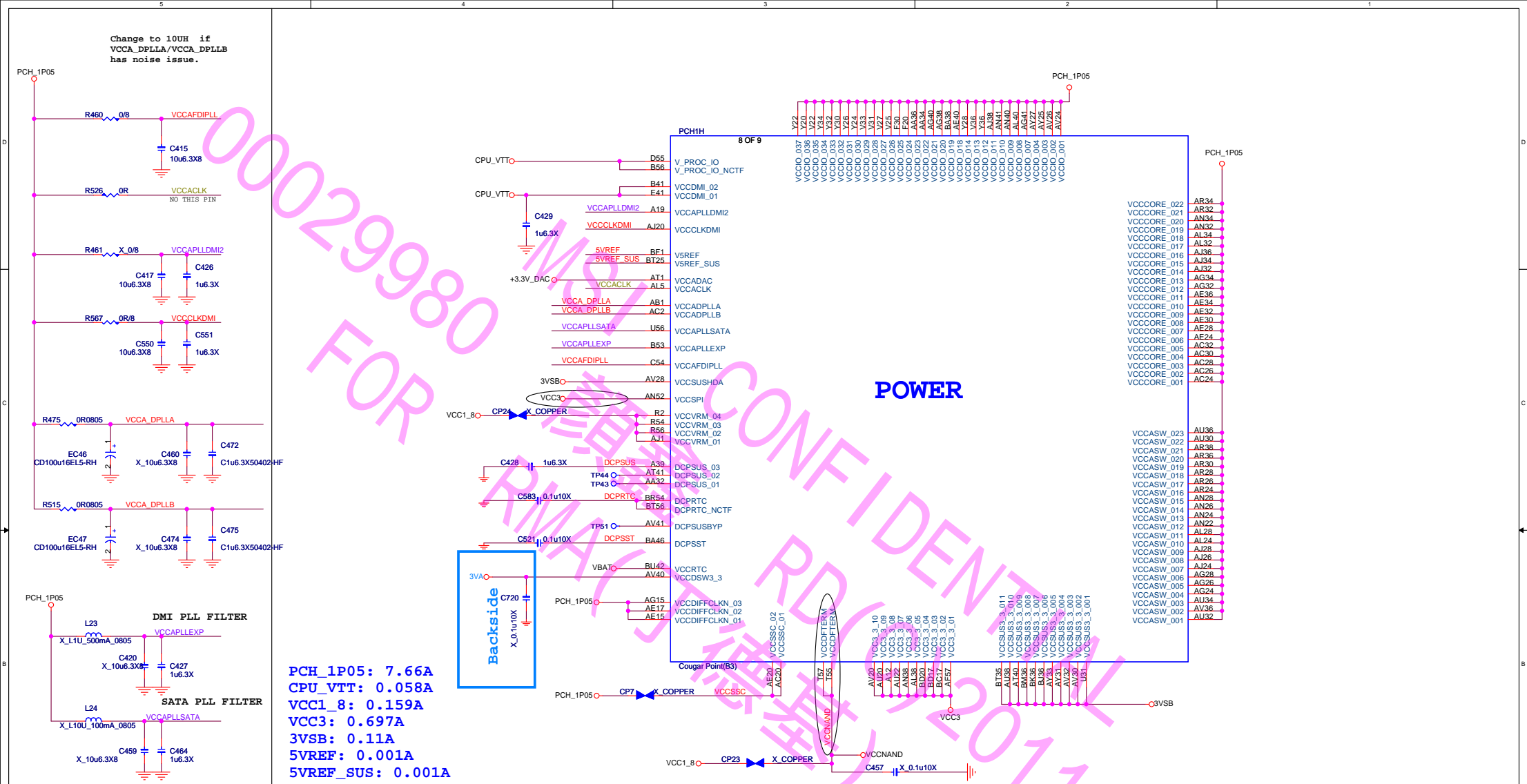
SPI FLASH ROM

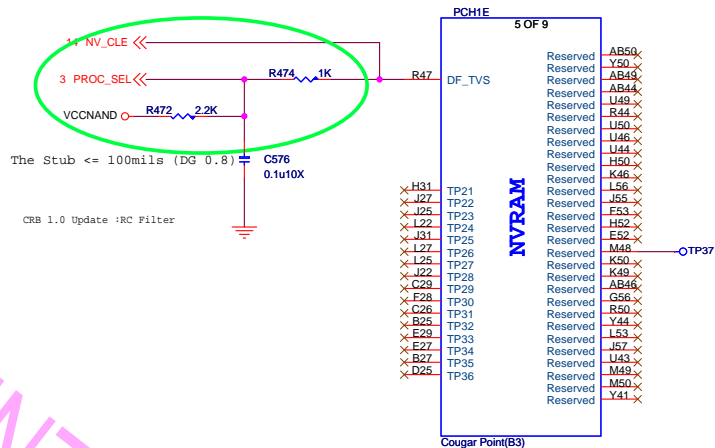
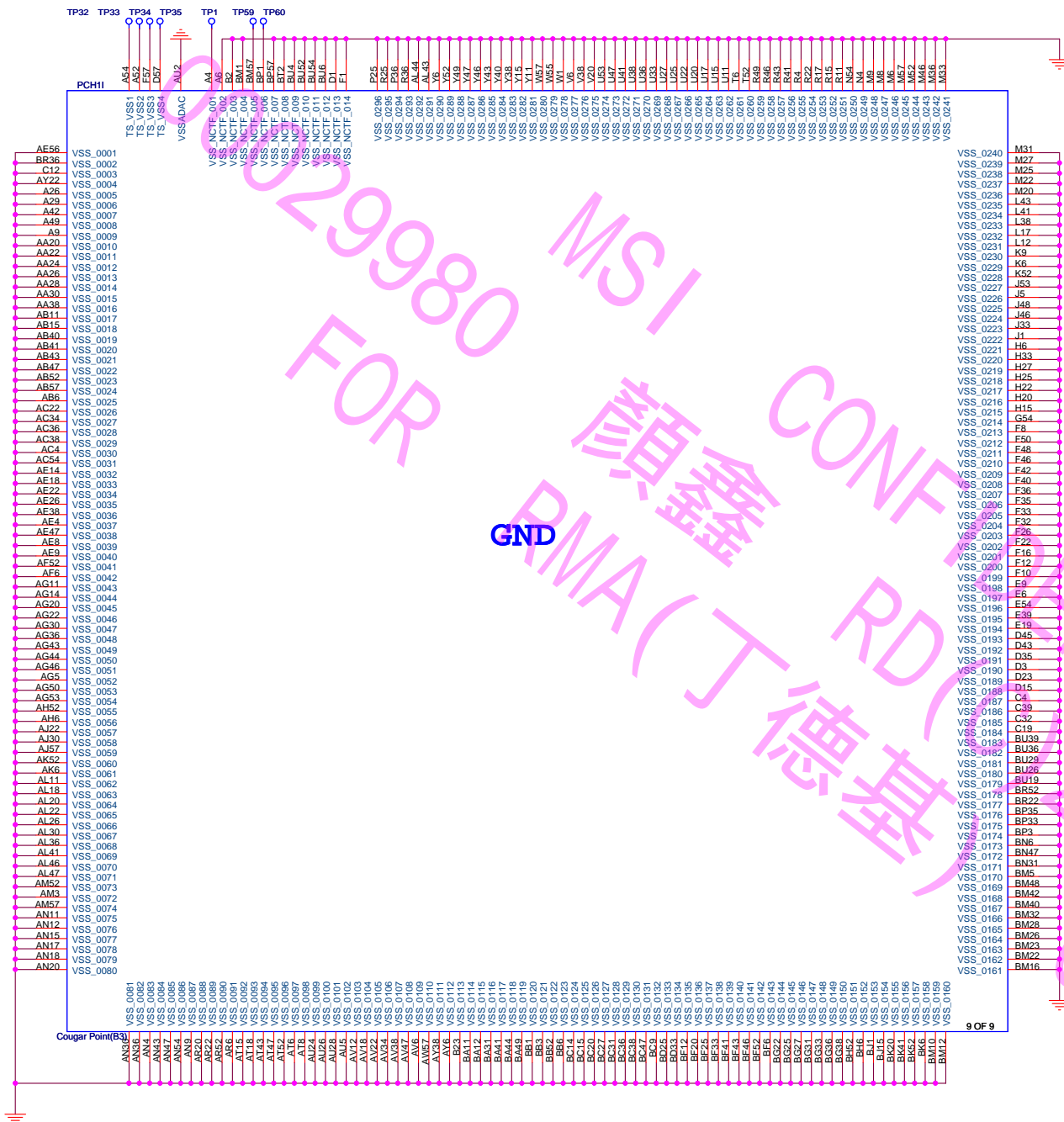
Place close to SB.



Reserved for BIOS control used

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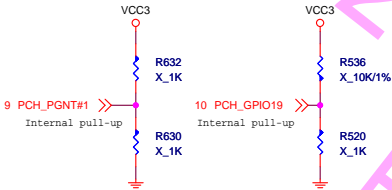
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Size Custom Document Description **CP-GND/NVRAM** Rev 4.1

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PCH Straps

BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	1	0
SPI	1	1



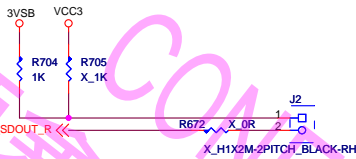
INTVRMEN
0: DISABLE INTERNAL VRM
1: ENABLE INTERNAL VRM *

When these voltage regulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.



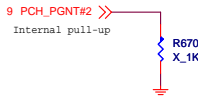
DSWVRMEN
0 : Disable Internal Deep Sleep 1.05 V regulators.
1 : Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V regulators. Must be reconnected even when not supporting DSW.

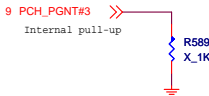


HDA_SDO
Disable ME in Manufacturing Mode when pull LOW ????

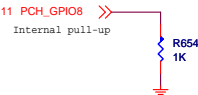
HDA_SDO has internal pull down.
Default should be connected to SDIN of codec, no pull up/down.
To Disable ME need to have a jumper to pull high



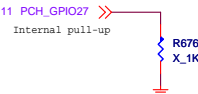
DMI AC/DC MODE
0 : AC
1 : DC *



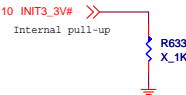
Topblock swap override when pull-low
Signal has a weak internal pull-up



GPIO8
0 : Integrated Clocking Enable (FCIM)*
1 : Buffer Through Mode Enable (BTM)

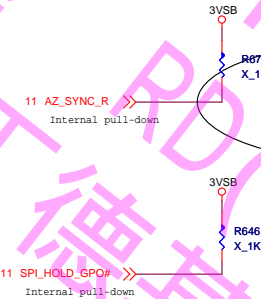


GPIO28
0 : OD PLL VR disabled
1 : OD PLL VR enabled *
Signal has a weak internal pull-up



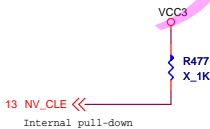
INT3_3V#
0 : ??????????????
1 : ?????????????? *

1: INIT3_3V to asserted for 16 PCI clock to reset the processor by some evens occur.
0: Can not to reset the processor.

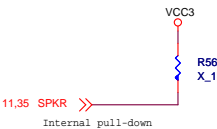


HDA_SYNC
OD PLL VR SUPPLY SEL
0: 1.8V SUPPLY *
1: 1.5V SUPPLY

GPIO15
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY *
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY



DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW *?
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP

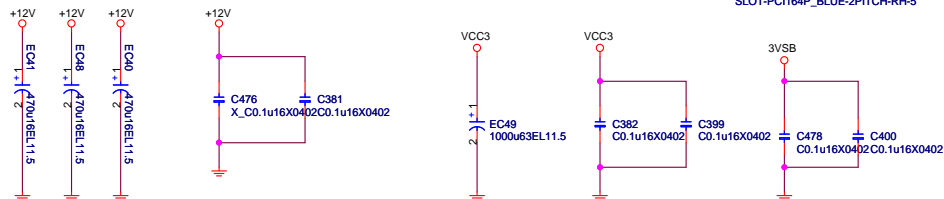
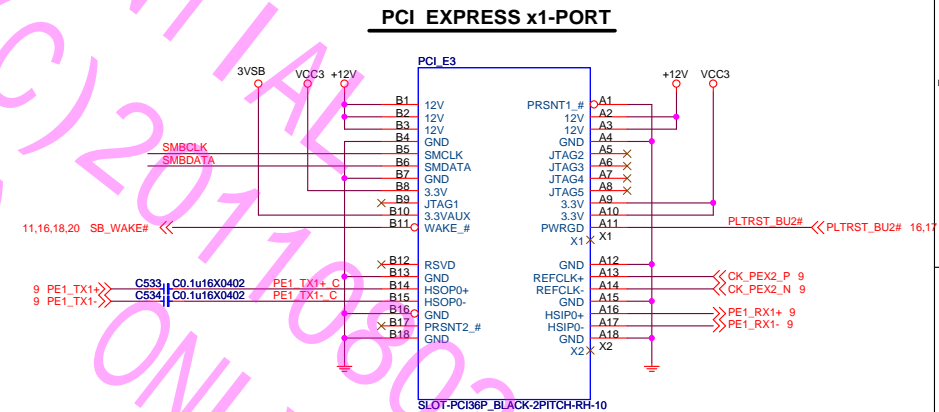
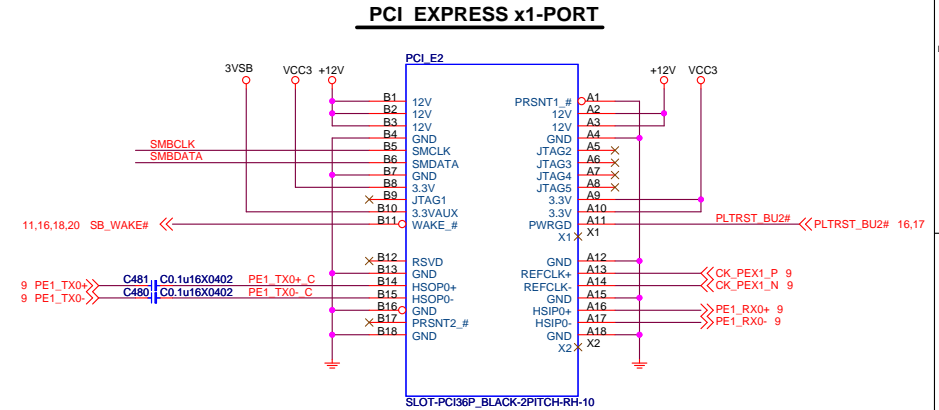


SPKR
0 : EN TCO REBOOT *
1 : DIS TCO REBOOT



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PCI_Express X16 Slot

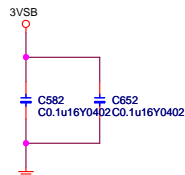
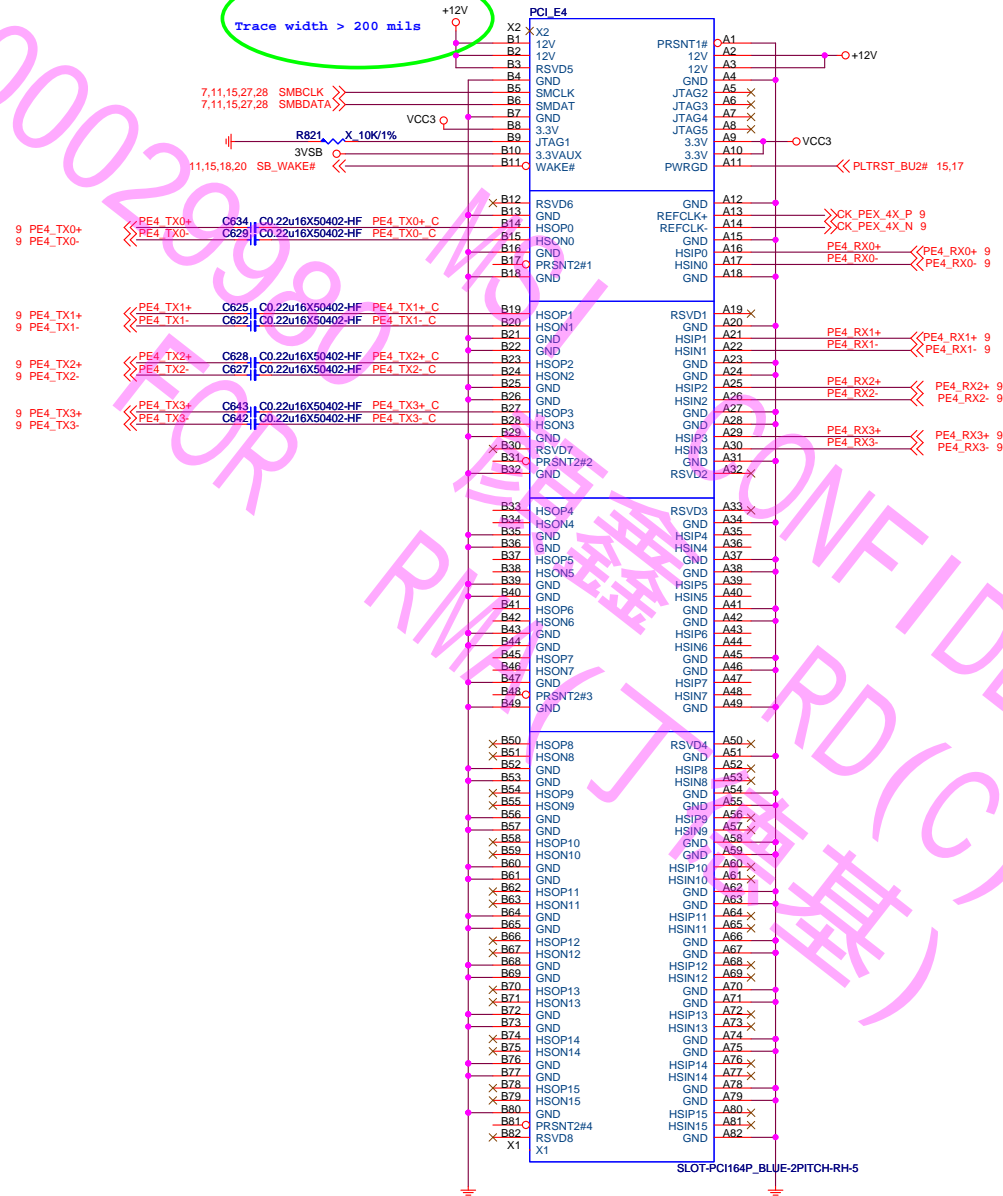


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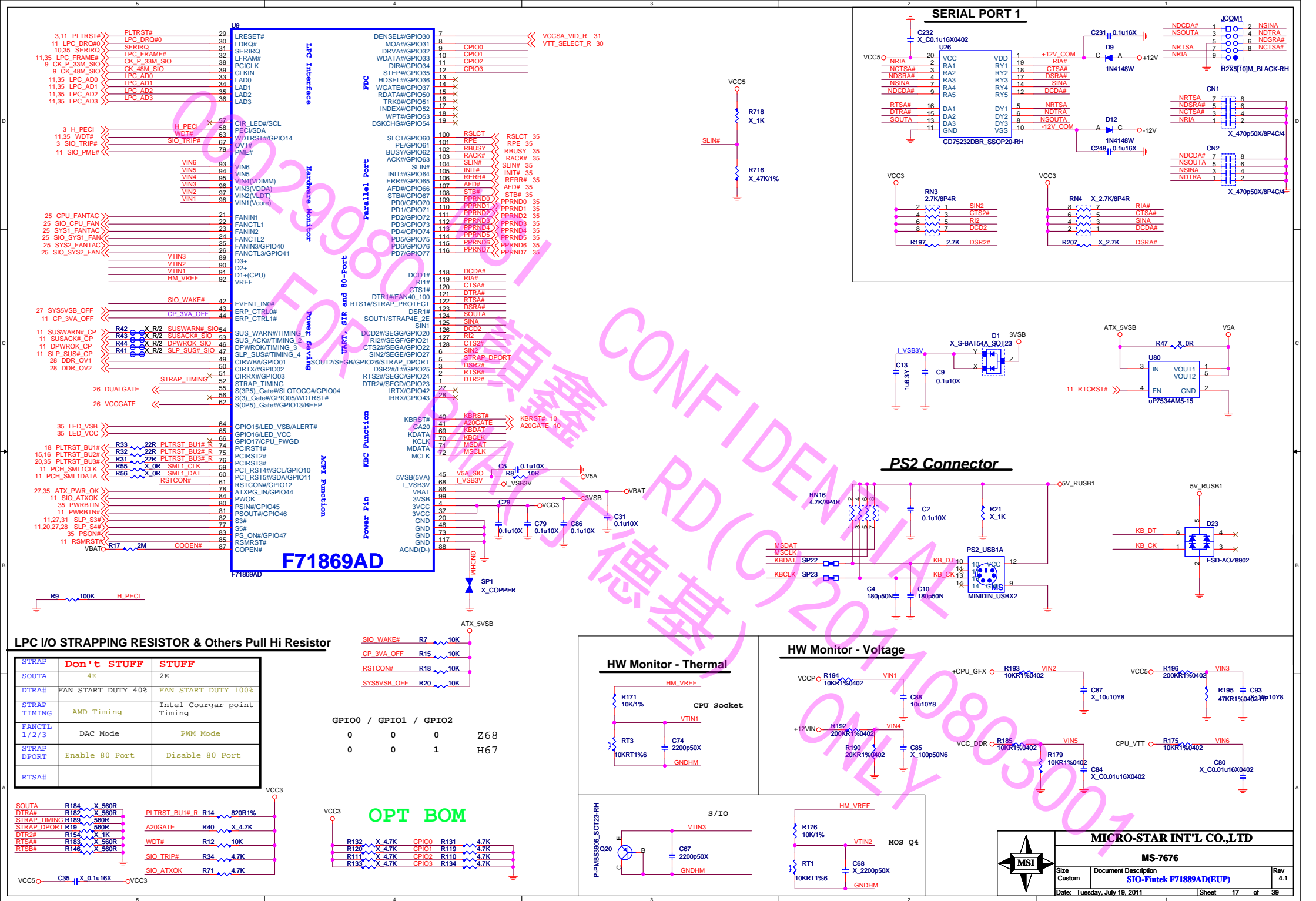
PCI_Express X4 Slot



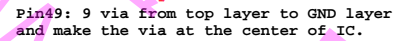
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RTL8105E 10/100M LAN



Place near pin

3VSB

CP14 X COPPER

CP6 X COPPER

VDD33

27 39 42 47 48 12

C436 X0/n1,0

C409 X0/n1,0

C407 X0/n1,0

C411 X0/n1,0

C410 X0/n1,0

C438 X0/n1,0

811E: stuff

8105E: unstuff

Place near pin

VDD10

3 13 19 45 41 6 9

C416 0.1u10X

C446 0.1u10X

C433 0.1u10X

C412 0.1u10X

C408 0.1u10X

C424 0.1u10X

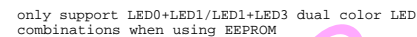
C435 0.1u10X

R Consumption

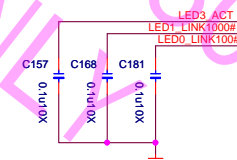
	3.3V	mW
811E: stuff		
8105E: unstuff		

	3.3V	mW
10 M Idle/TxRx	14/75	46/248
100 M Idle/TxRx	43/66	142/218
S0 ALDPS	3.2	11

	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13

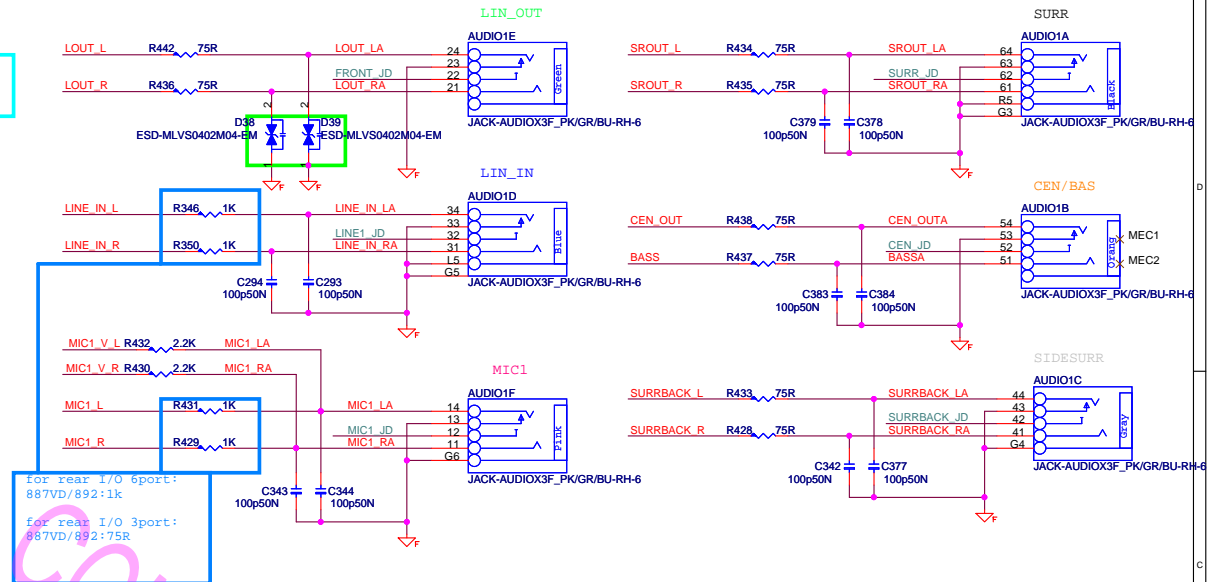
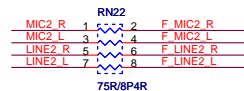
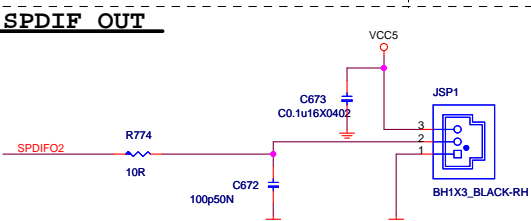
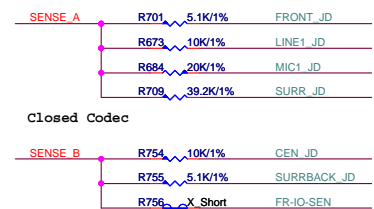
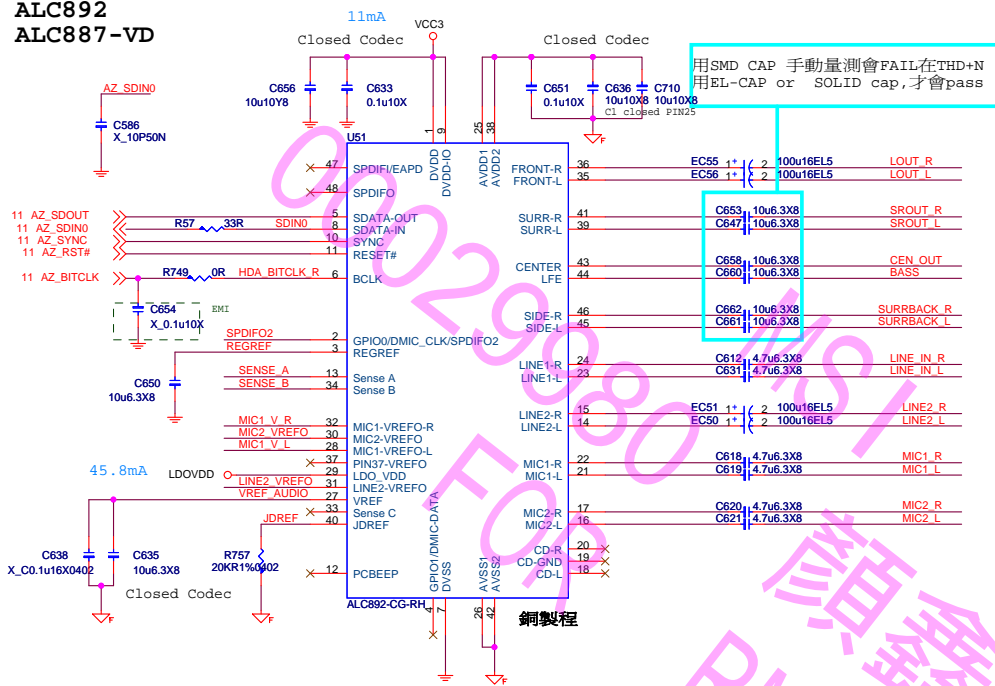


Giga-Lan	10/100-Lan
<p>N58-22F0731</p> <p>Link Yellow Active Blinking 1000 Orange 100 Green 10 None</p>	<p>N58-22F0771</p> <p>Link Yellow Active Blinking 100 Green 10 None</p>

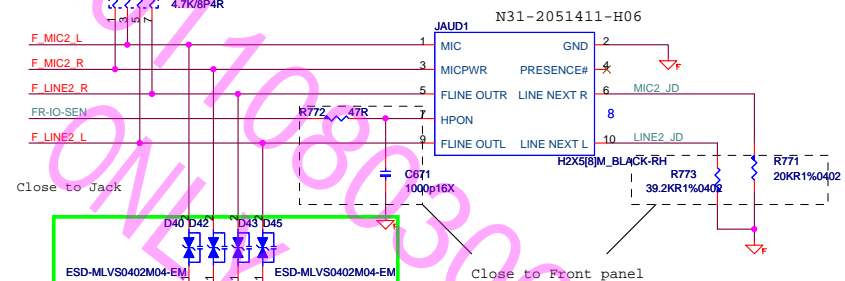
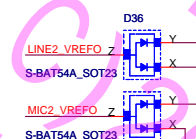


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ALC892
ALC887-VD



當串接電容有極性時，
需上對地電阻

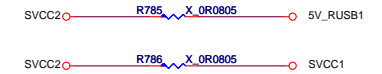
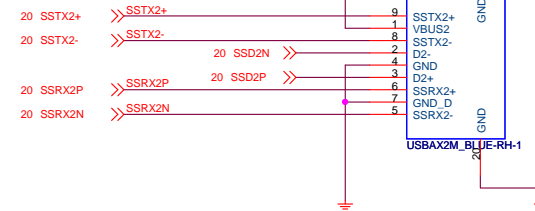
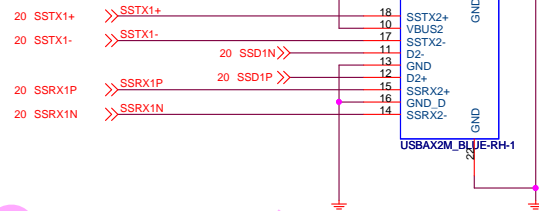


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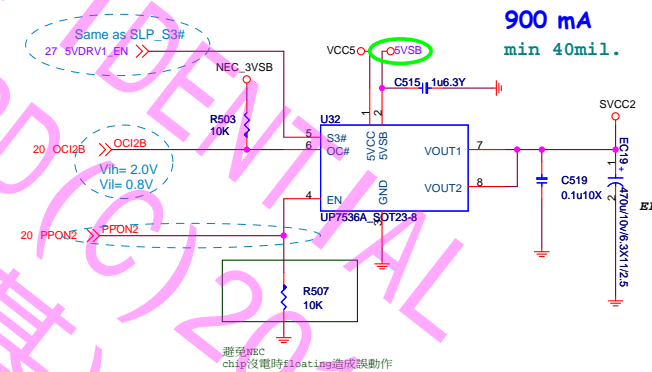
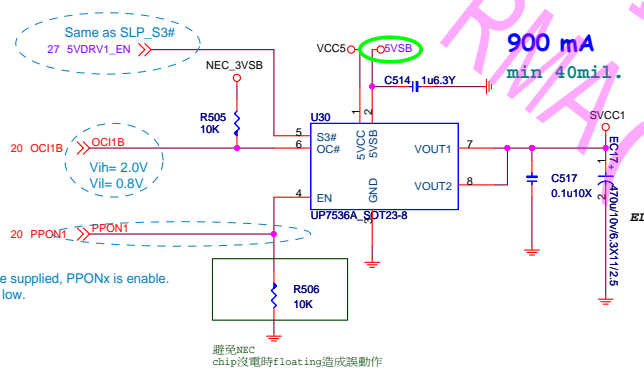
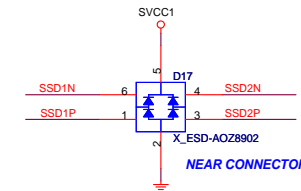
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Rear I/O



ESD Protection

Close to Connector

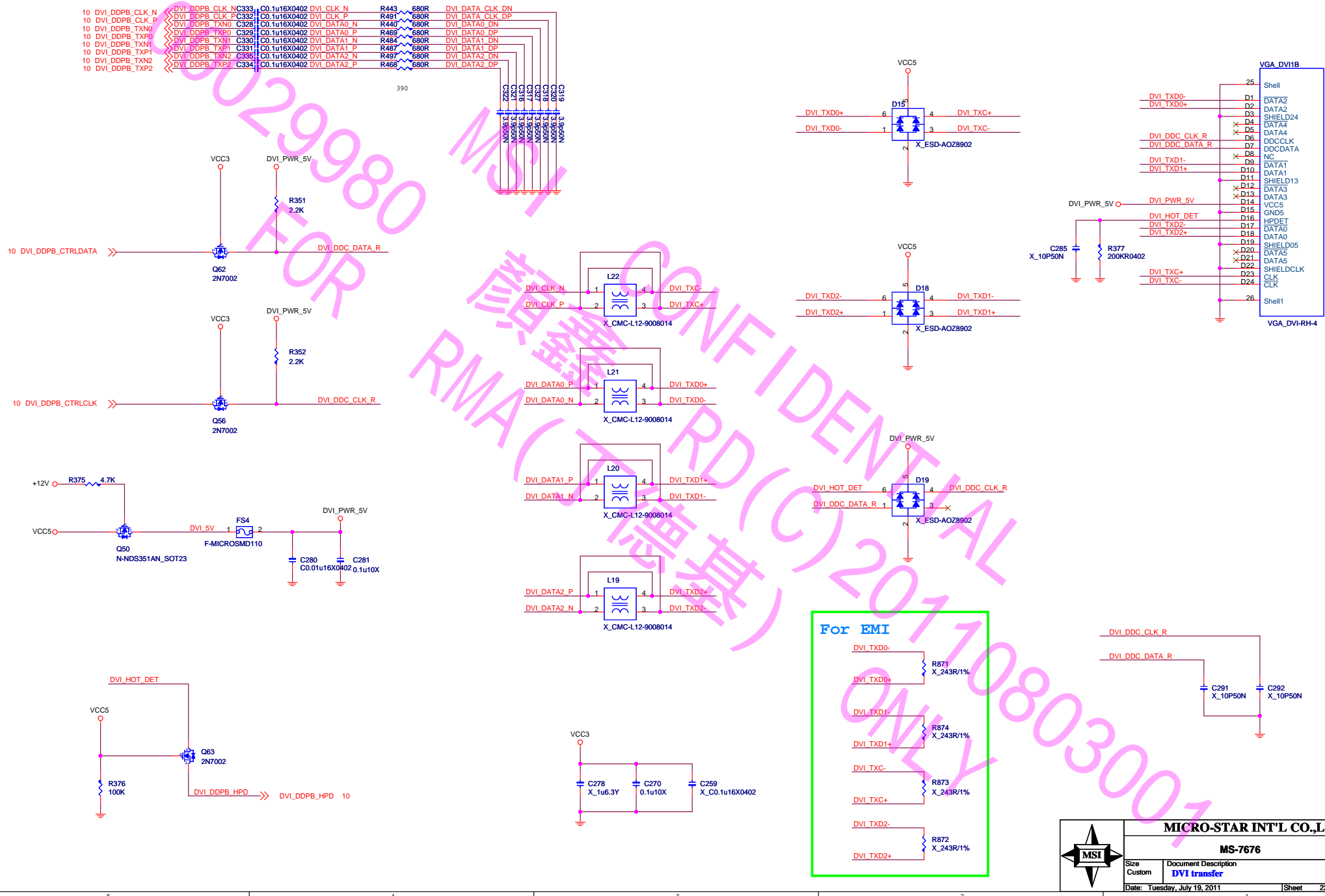


All power sources of uPD720200 are supplied, PPNx is enable.
PPONx is low when OCx going to low.

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DVI level shifter

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



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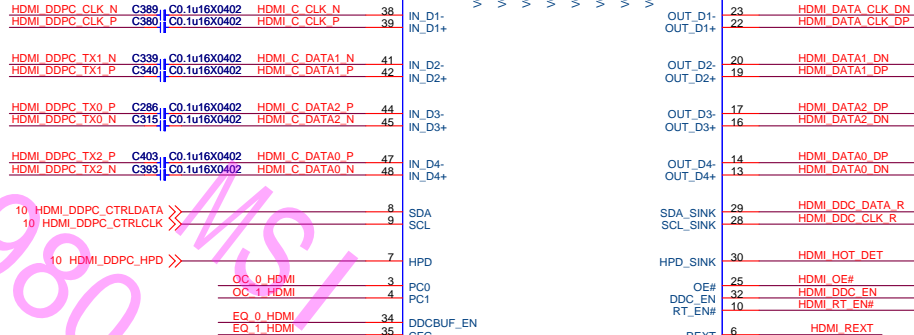
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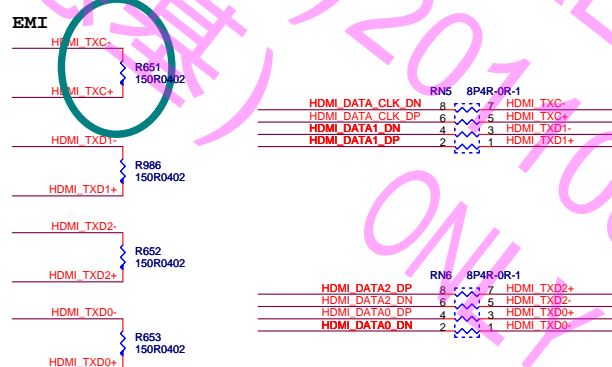
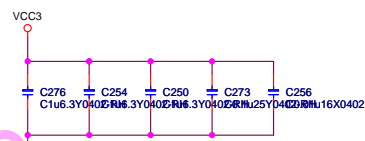
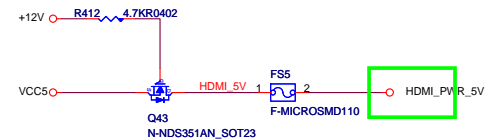
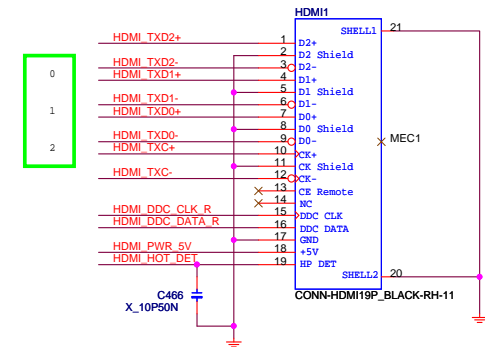
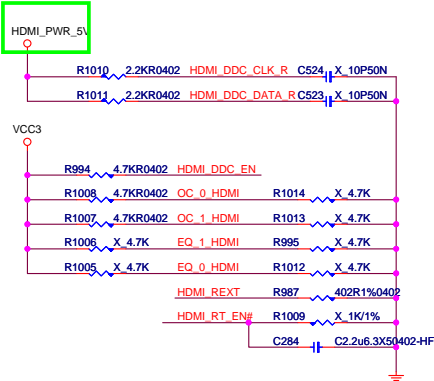
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HDMI level shifter

10 HDMI_DDPC_CLK_P << HDMI_DDPC_CLK_P
10 HDMI_DDPC_CLK_N << HDMI_DDPC_CLK_N
10 HDMI_DDPC_TX2_P << HDMI_DDPC_TX2_P
10 HDMI_DDPC_TX2_N << HDMI_DDPC_TX2_N
10 HDMI_DDPC_TX1_P << HDMI_DDPC_TX1_P
10 HDMI_DDPC_TX1_N << HDMI_DDPC_TX1_N
10 HDMI_DDPC_TX0_P << HDMI_DDPC_TX0_P
10 HDMI_DDPC_TX0_N << HDMI_DDPC_TX0_N




PERICOM料號: B0B-411LS2C-P22.
PARADE料號: B0B-081010C-P97.



	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer	PC1, PC0		note
1, 0, X	On	Off	00	8 dB	internal pull-down at ~500K ohm.
1, 1, 0	Off	On	01	4 dB	
1, 1, 1	Off	Off	10	12 dB	
0, X, X	Off	Off	11	0 dB	



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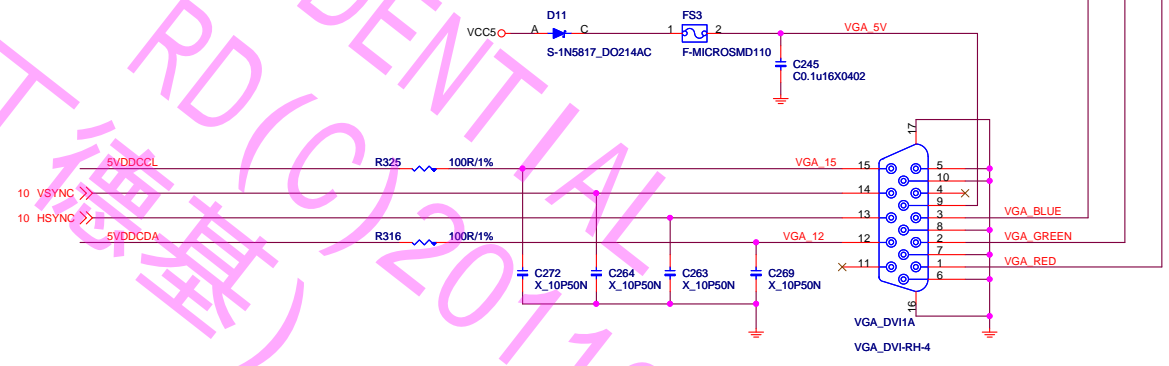
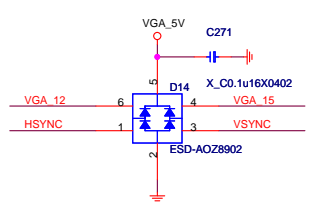
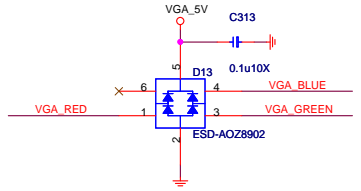
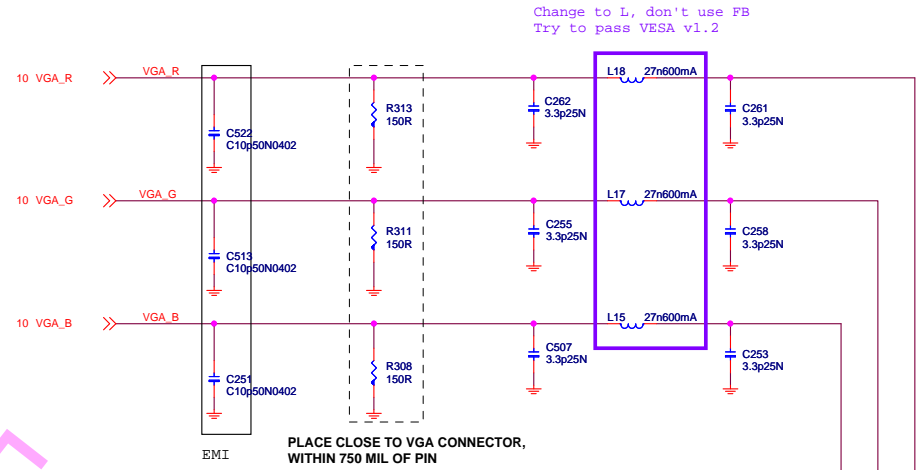
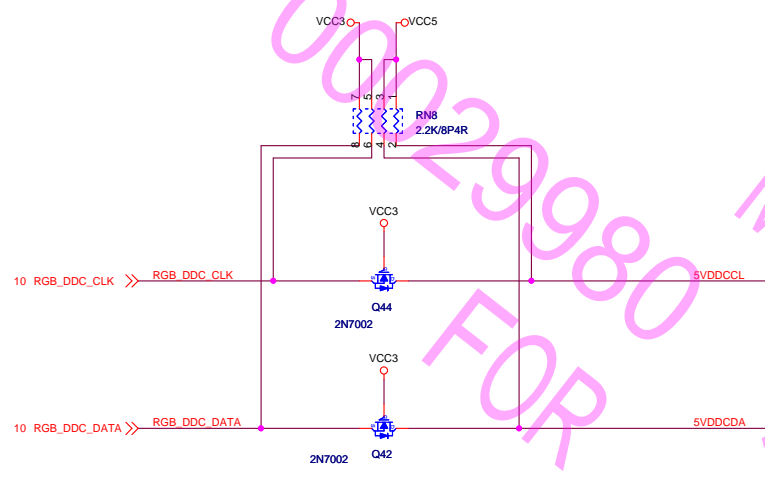
MS-7676


Size Custom	Document Description HDMI	Rev 4.1
Date: Tuesday, July 19, 2011	Sheet 23 of 39	

D-Sub

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

Level shift

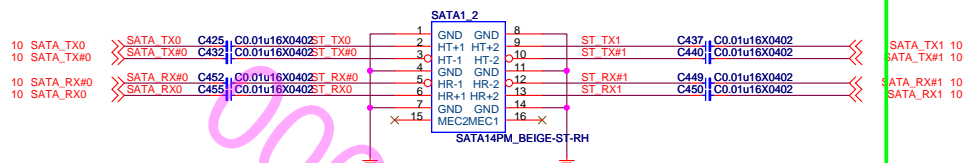




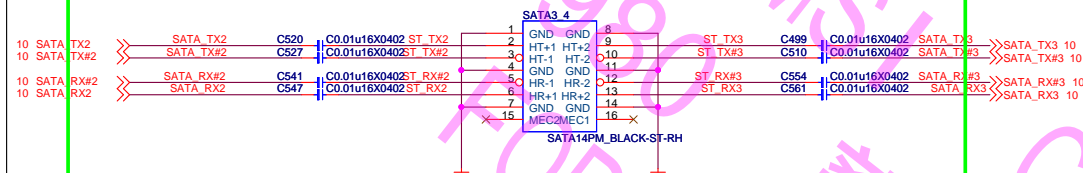
MICRO-STAR INT'L CO.,LTD		
MS-7676		
Size	Document Description	Rev
Custom	VGA	4.1
Date: Tuesday, July 19, 2011		Sheet 24 of 39

SATA 6G PORT 0,1

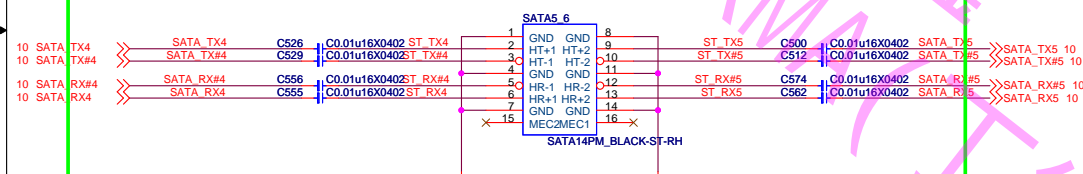
H61 PORT 0/1 Support 3G
H67 PORT 0/1 Support 6G



SATA 3G PORT 2,3

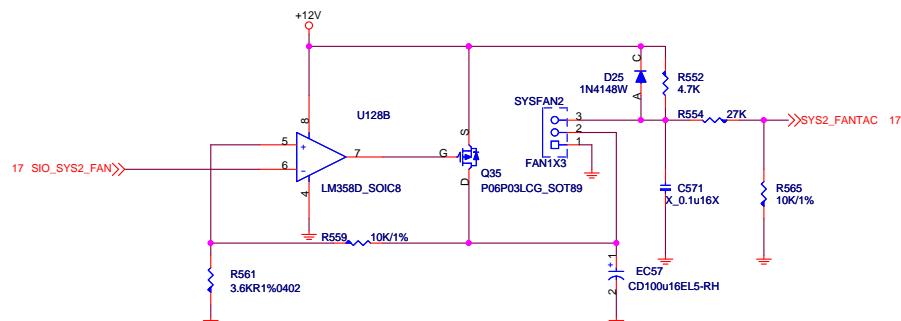


SATA 3G PORT 4,5

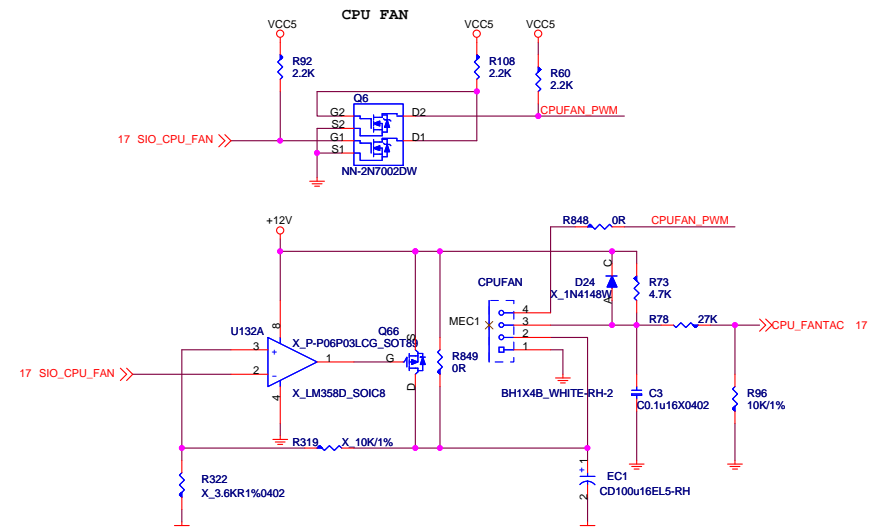


SYSTEM FAN-COUNT CONTROL CIRCUIT

SYSTEM FAN2

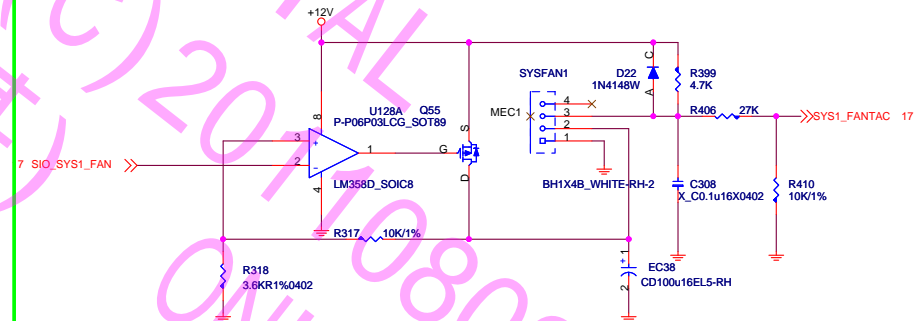


CPU FAN-COUNT CONTROL CIRCUIT



SYSTEM FAN-COUNT CONTROL CIRCUIT

SYSTEM FAN1

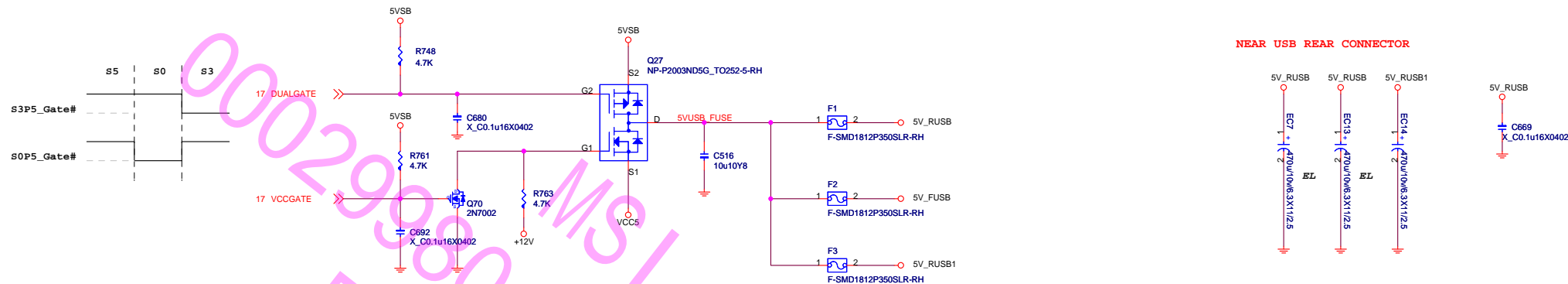


MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	SATA / FAN Control	4.1
Date: Tuesday, July 19, 2011	Sheet 25 of 39	

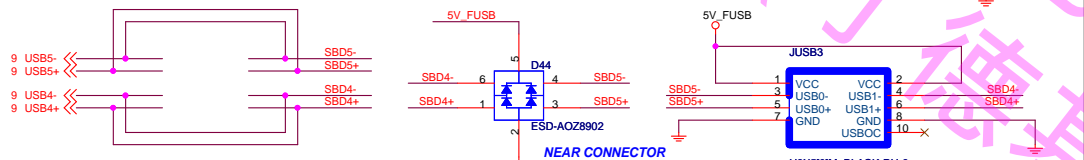
5V_RUSB Switch



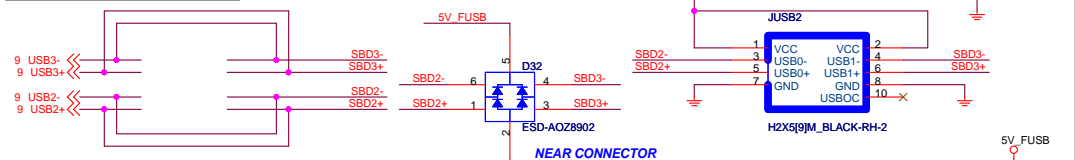
Front USB Connector

For H61 6,7,12,13 Port should be remove

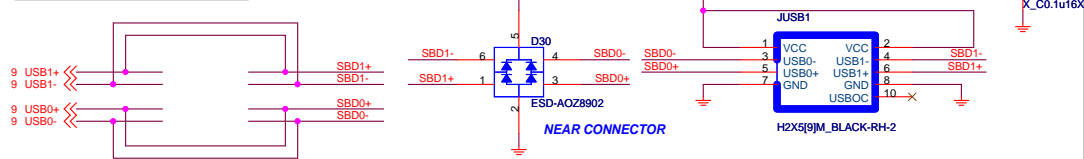
FRONT USB PORT 4,5



FRONT USB PORT 2,3

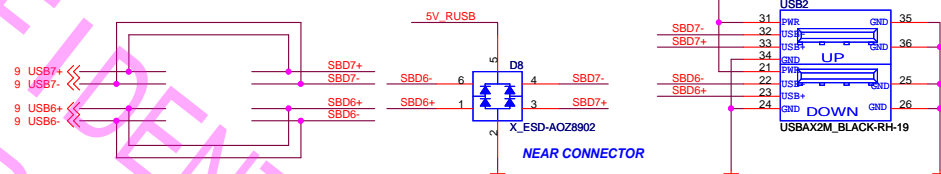


FRONT USB PORT 0,1

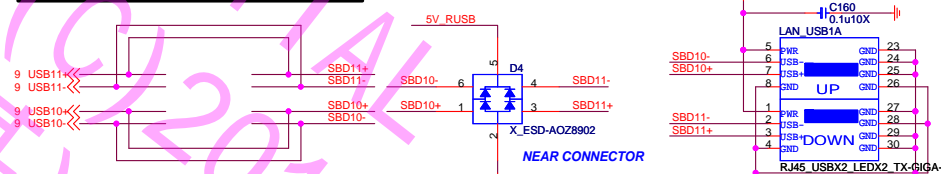


Rear USB Connector

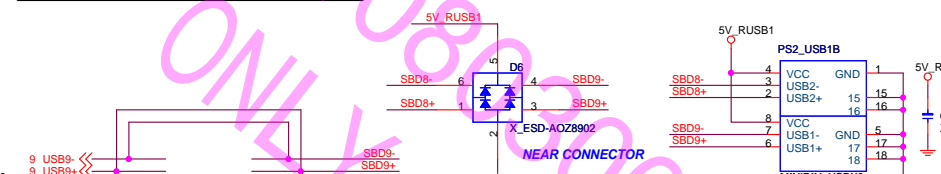
REAR USB PORT 6,7 (With HDMI)



REAR USB PORT 10,11 (With LAN)



REAR USB PORT 8,9 (With PS2)

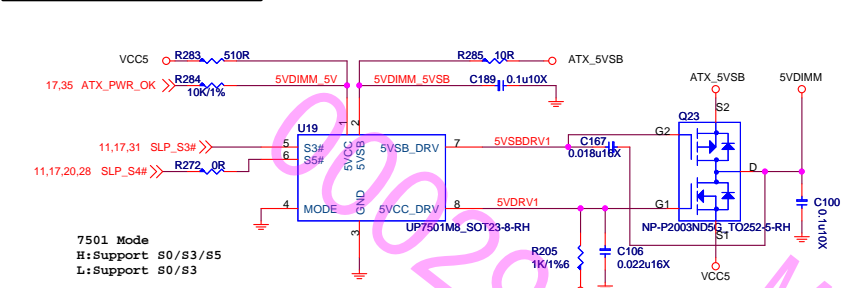


MICRO-STAR INT'L CO.,LTD

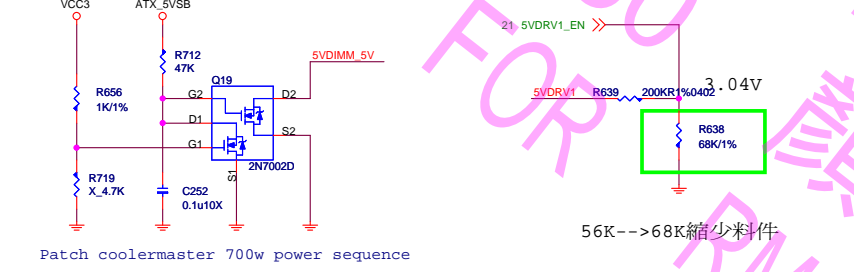
MS-7676

Size	Document Description	Rev
Custom	USB Connector	4.1
Date: Tuesday, July 19, 2011	Sheet 26 of 39	

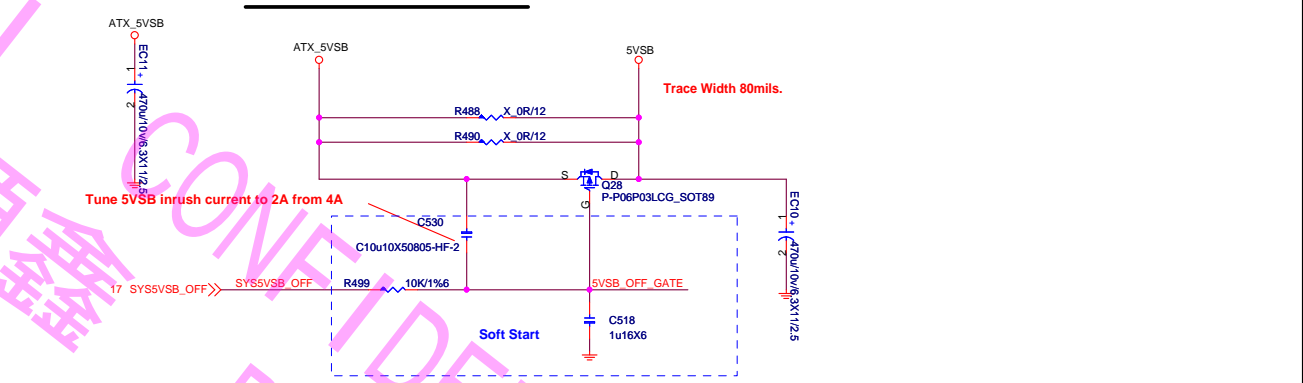
5VDIMM FOR DDR



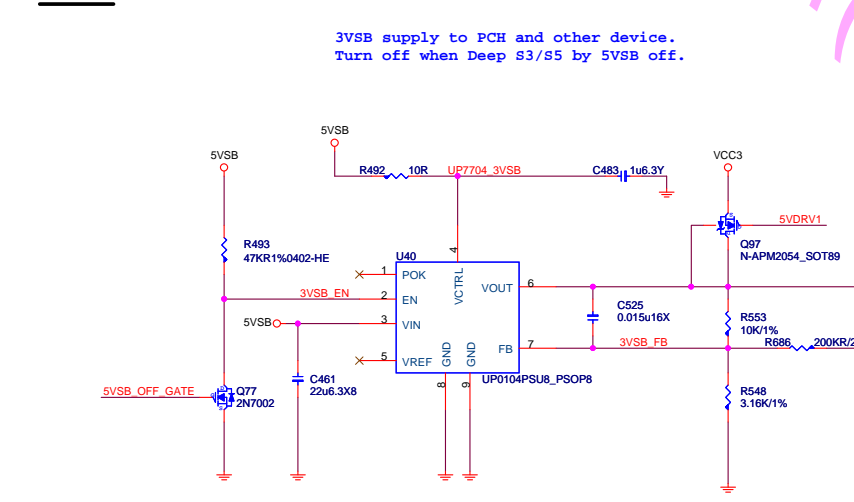
USB MODE



5VSB Power Switch



3VSB



UPI VOLTAGE CONSOLE

0x2A: RL=10K, RH=OPEN

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%



MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	ACPI controller UPI	4.1

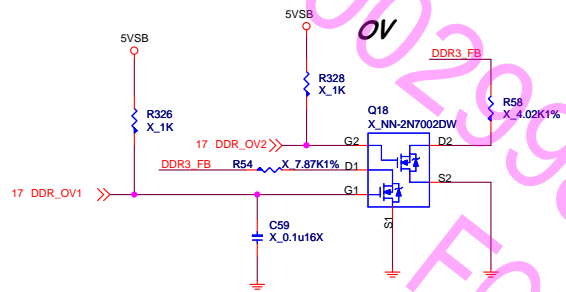
Date: Tuesday, July 19, 2011 | Sheet 27 of 39

DDR3_1.5V 4.5A+7.5A+1A=13A

4.5A FOR CPU

7.5A FOR 2DIMM

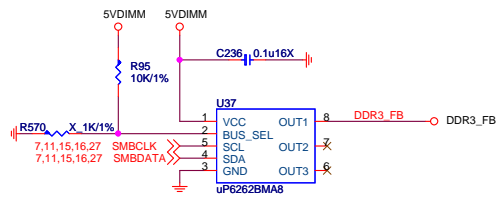
1A FOR DDR VTT



*Default 1.5V

DDR_OV	1.35V	1.5V	1.65V	1.8V
DDR_OV1	Low	High	Low	High
DDR_OV2	Low	Low	High	High

DDR_OV1 = GPIO01 (S/I/O)
DDR_OV2 = GPIO02 (S/I/O)

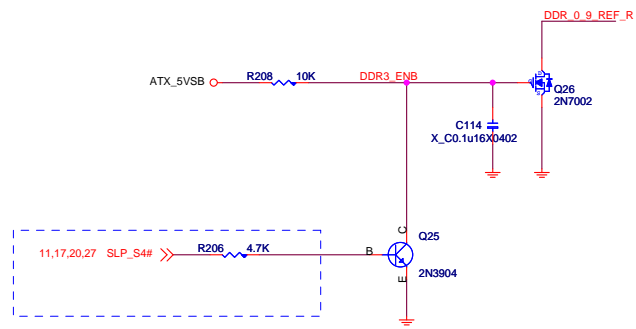


UPI VOLTAGE CONSOLE

0x20: RH=1.0K, RL=OPEN

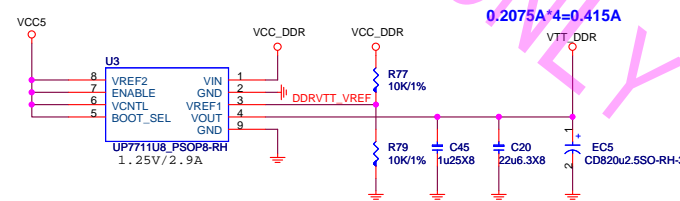
ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

P.S. Only for meet Intel power down sequence.



DDR VTT Power

To CPU Copper trace width > 250mils, Fill island behind DIMM > 400mils.



MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	DDR Power - uP6103 1-Phase	4.1
Date:	Tuesday, July 19, 2011	Sheet 28 of 39

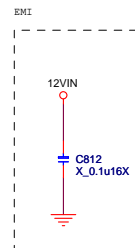
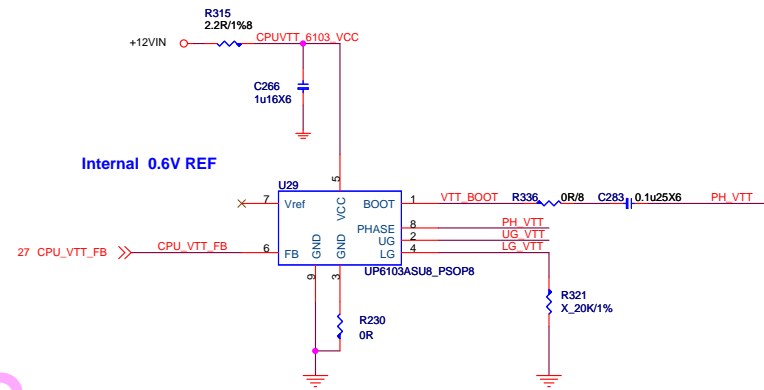
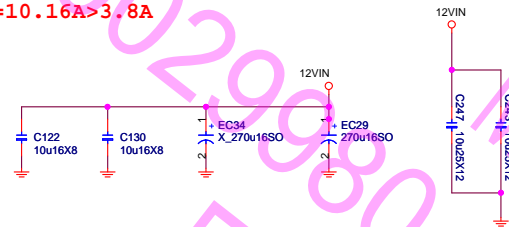
1.8A FOR ME CORE



CPU_VTT:1.05/1.00

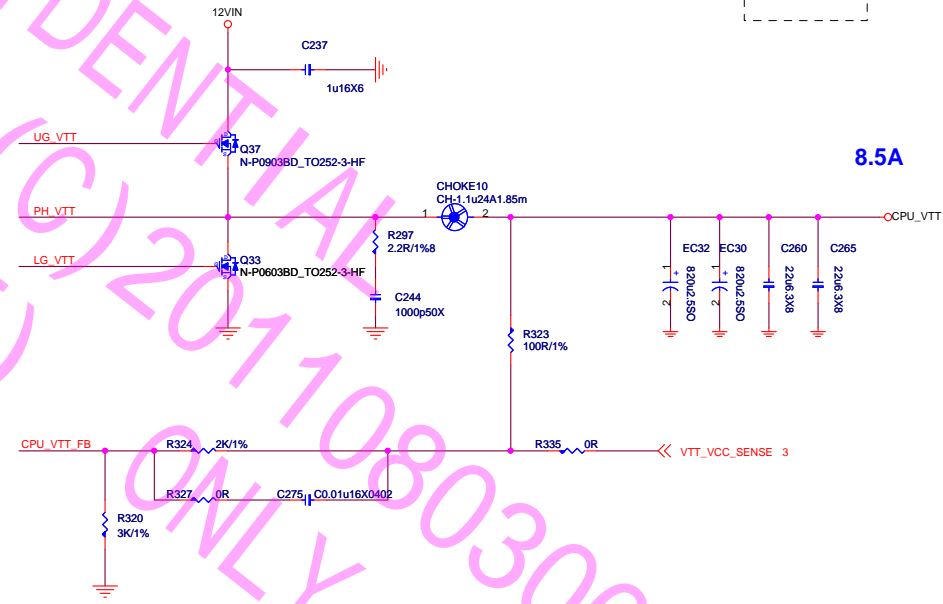
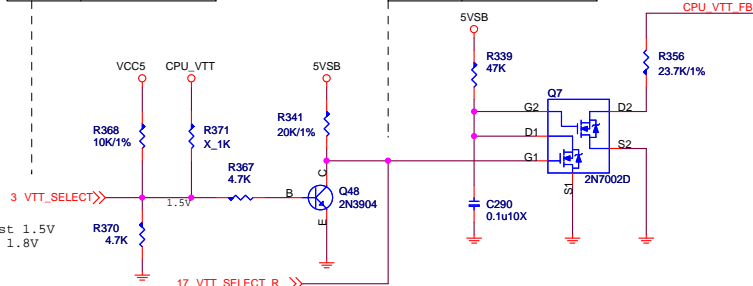
CPU VTT 8.5A + SA Core =8.8A =17.3A


$I_{ripple} = 1.92(vtt) + 1.88(sa)$
 $5.08 * 2 = 10.16A > 3.8A$



VTT_SELECT	
Low	1.0V
High	1.05V

VTT_SELECT Table	
Low	1.05V
High	1.0V





MICRO-STAR INT'L CO.,LTD

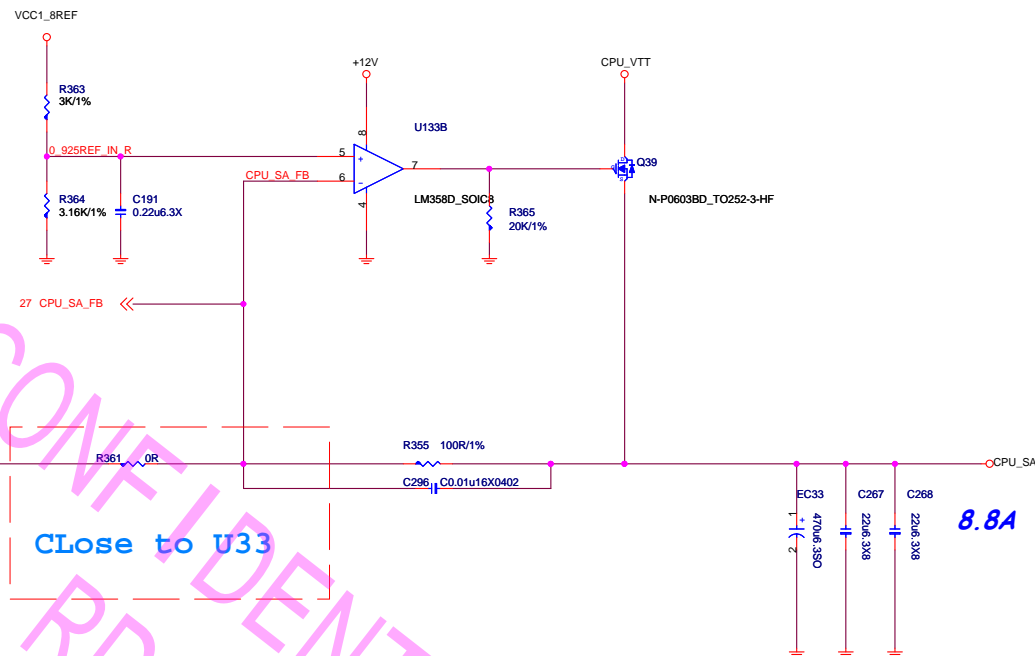
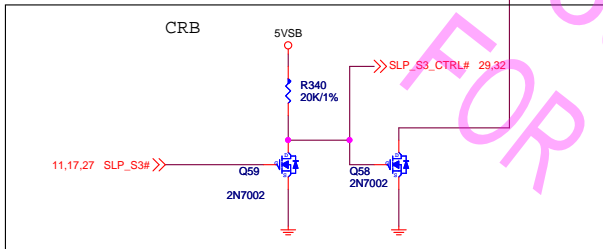
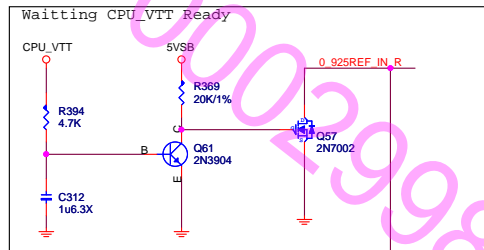
MS-7676

Size Custom Document Description **CPU_VTT - uP6103- 1-Phase** Rev 4.1

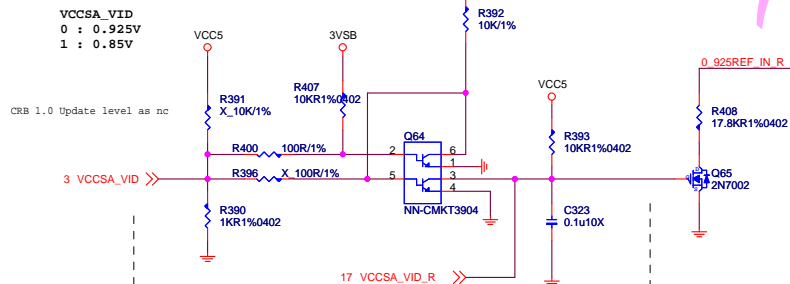
Date: Tuesday, July 19, 2011 Sheet 30 of 39

CPU_SA:0.925/0.85

SA Core =8.8A



Close to U33



VCCSA_VID	
Low	0.925V
High	0.85V

VCCSA_VID_SIO Table	
Low	0.925V
High	0.85V

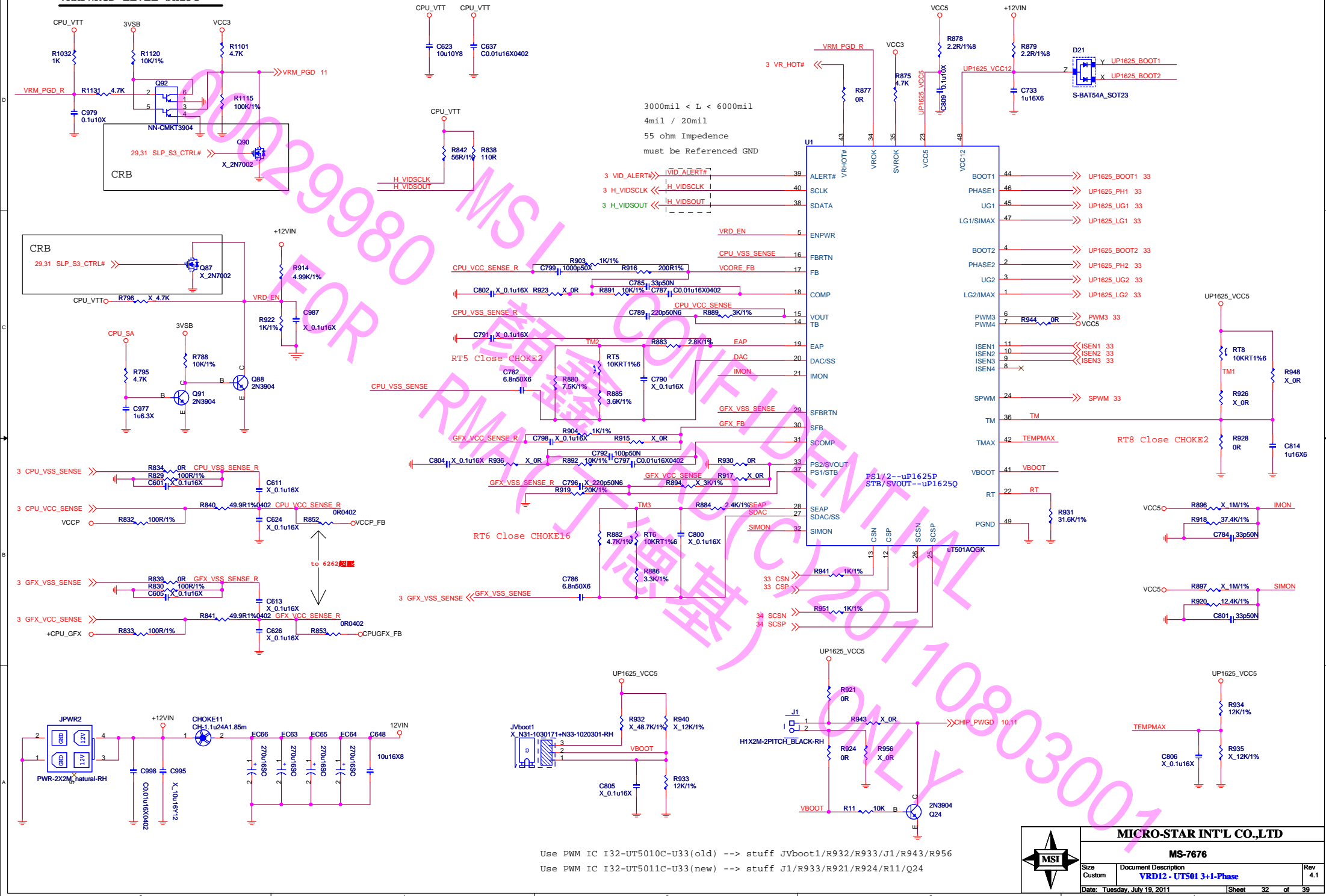


MICRO-STAR INT'L CO.,LTD

MS-7676

Size	Document Description	Rev
Custom	CPU_SA - uP6103 1-Phase	4.1
Date:	Tuesday, July 19, 2011	Sheet 31 of 39

VRMPWRGD LEVEL SHIFT



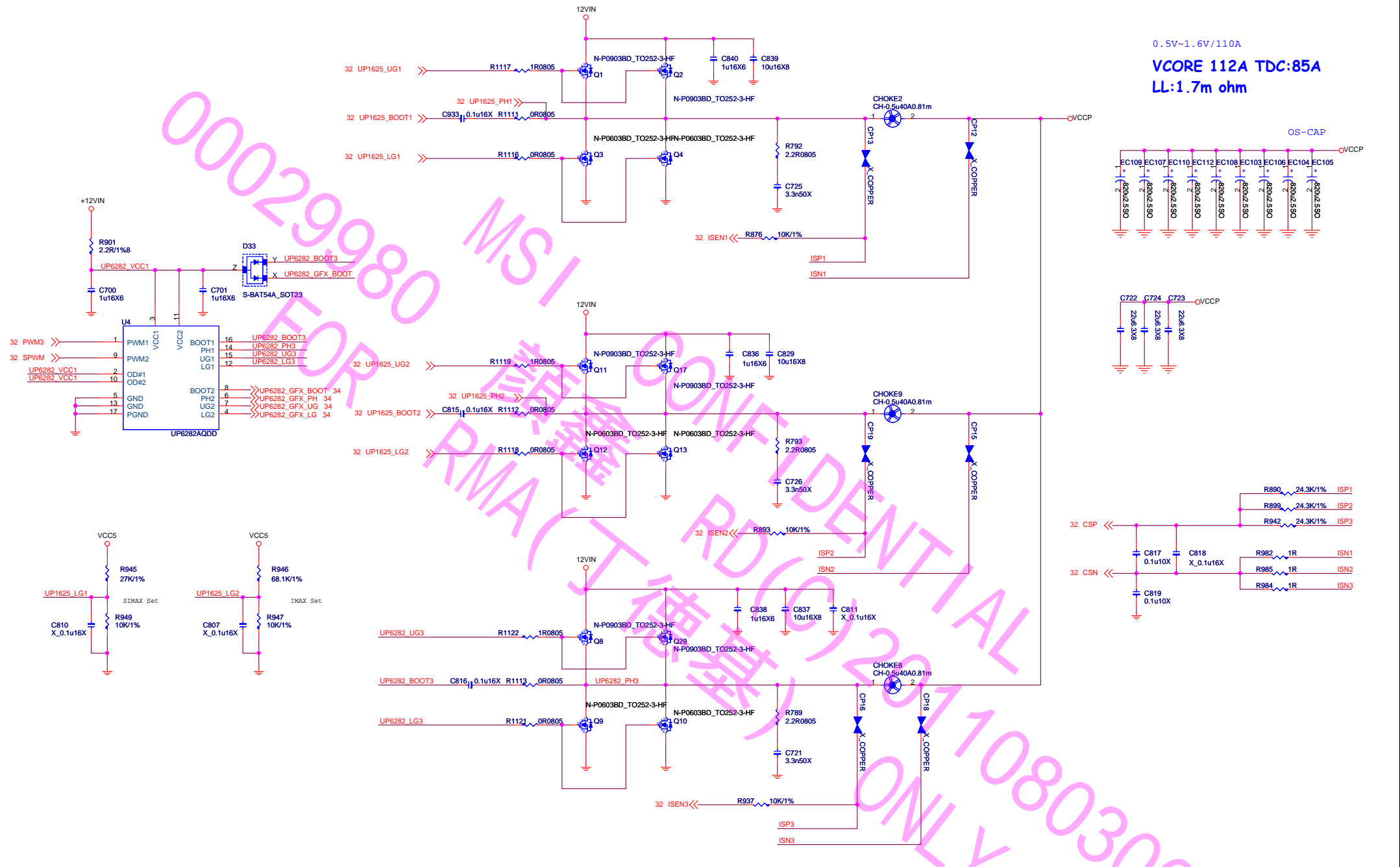
```
Use PWM IC I32-UT5010C-U33(old) --> stuff JVboot1/R932/R933/J1/R943/R956
Use PWM IC I32-UT5011C-U33(new) --> stuff J1/R933/R921/R924/R11/Q24
```



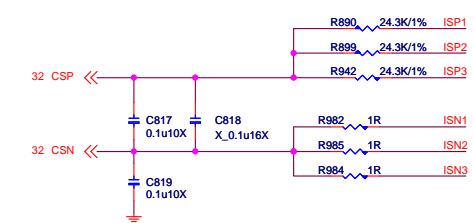
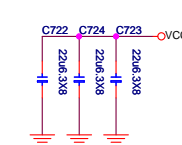
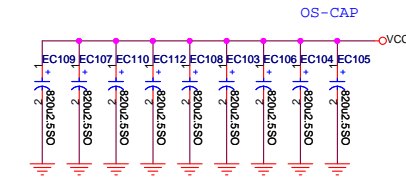
MICRO-STAR INT'L CO.,LTD

MS-7676

Size Custom	Document Description VRD12 - UT501 3+1-Phase	Rev 4.1
Date: Tuesday, July 19, 2011		Sheet 32 of 39

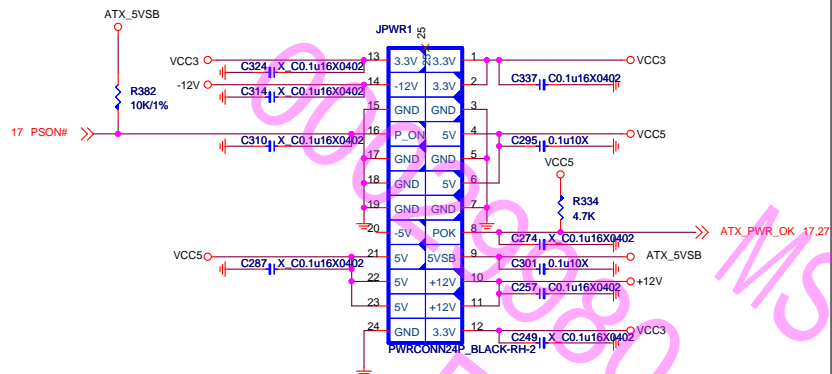


0.5V~1.6V/110A
VCORE 112A TDC:85A
LL:1.7m ohm

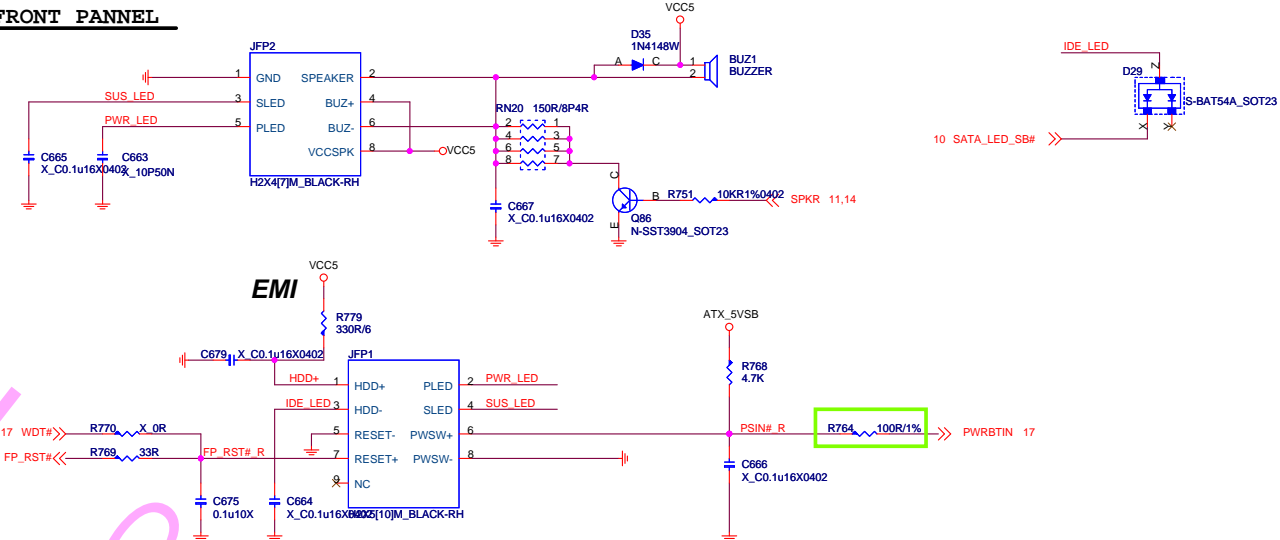


MICRO-STAR INT'L CO.,LTD			
MS-7676			
Size	Document Description	Rev	
Custom	UP6282 3-Phase CPU	4.1	
Date: Tuesday, July 19, 2011		Sheet	33 of 39

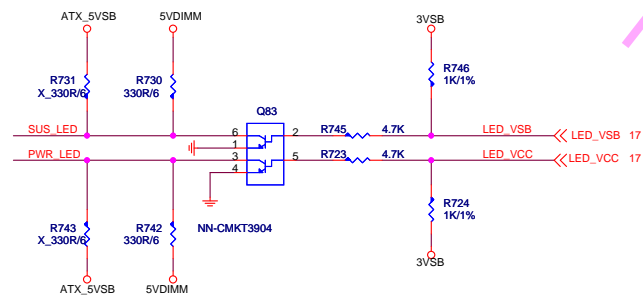
ATX POWER CONNECTOR



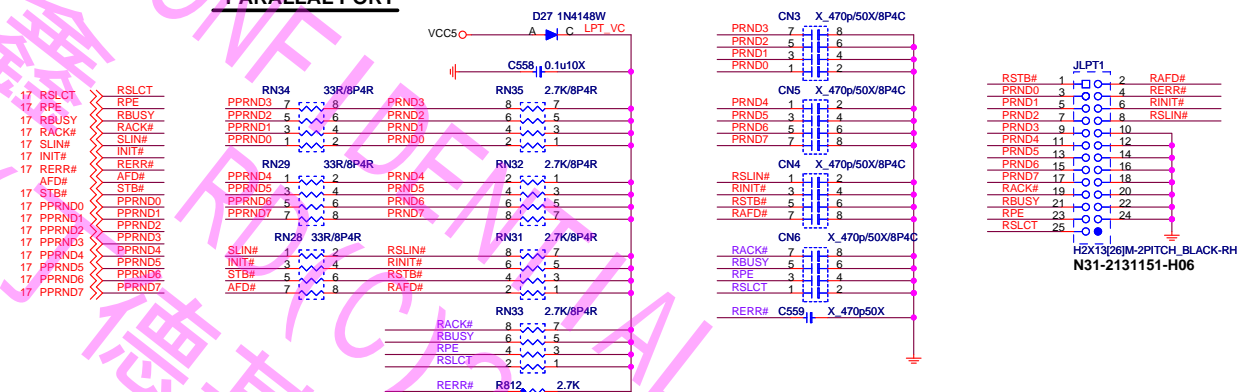
FRONT PANNEL



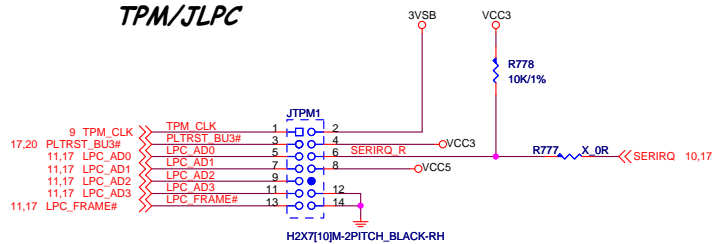
LED (for Fintek 71869)



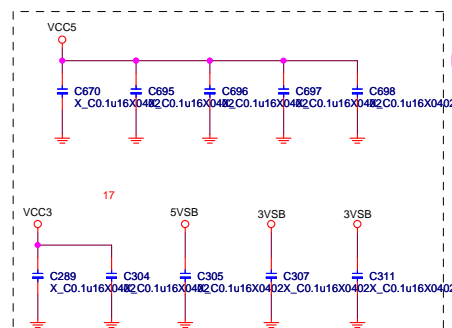
PARALLAL PORT



TPM/JLPC



EMI



MICRO-STAR INT'L CO.,LTD

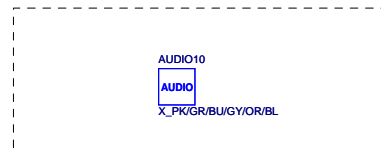
MS-7676

Size	Document Description	Rev
Custom	ATX PWR-Connector & Front Panel & EMI	4.1
Date: Tuesday, July 19, 2011	Sheet 35 of 39	

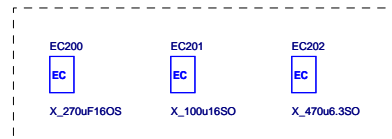
MS-7676-4.1

OPT	Configure	BOM	Function
	Z68 (B3)	601-7676-08S	MS-7676 4.1 Z68MA-G43 (B3), Z68 B3, 4*DDRIII, 2*PCIEx16+2*PCIEx1, Gb Lan, 4*SATAII+2*SATAIII, 2USB3.0+12*USB2.0, HD8Ch Audio, HDMI/DVI/D-sub, All Solid Cap, EuP, RoHS
A	H67 (B3)	601-7676-09S	MS-7676 4.1 OPT:A H67MA-G43 (B3), H67 B3, 4*DDR3, 2*PCIEx16+2*PCIEx1, G Lan, 4*SATA2+2*SATA3, 2USB3.0+12*USB2.0, HD8Ch Audio, HDMI/DVI/D-sub, All Solid Cap, EuP, RoHS

AUDIO CON OPT.



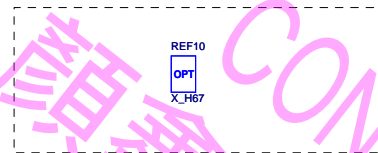
EL/OS OPT.



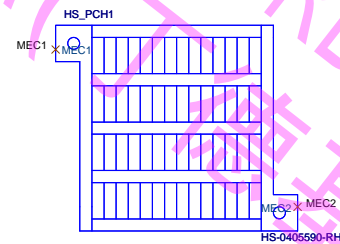
LABEL OPT.



SB



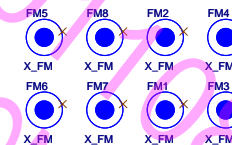
PCH XDP PWRGD/RESET



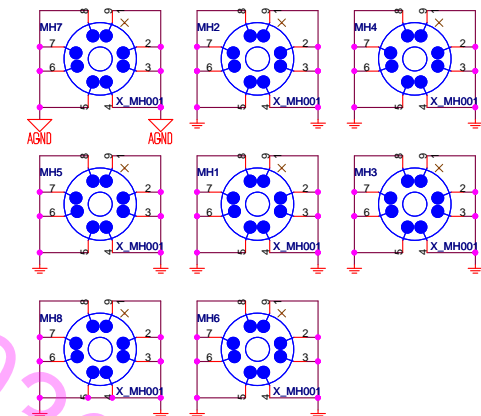
Simulation



Optical Fiducial Marks-120



Mounting Holes



7676-4.1



BAT-BCR2032P-RH



RUB1



RUB2

CPU 載座
E21-7557050-L06

HDMI LABEL



THX LABEL



VIRTU LABEL



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Size	Document Description	Rev
Custom	XDP / Manual Parts	4.1
Date: Thursday, July 21, 2011	Sheet 36 of 39	